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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,118	11/18/2003	Katsumi Shibayama	046124-5179	2756

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EXAMINER	
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2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/715,118	SHIBAYAMA ET AL.	
	Examiner	Art Unit	
	STEVEN H. RAO	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *17-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1, 3-16 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114.

Applicant's submission filed on 02/06/08 has been entered.

Therefore Claims 1-25 as previously recited and currently newly added claim 26 are pending in the Application.

Claims 17 to 25 have been with drawn from consideration.

Claim 2 has been cancelled.

Information Disclosure Statement

No further Ids after the one filed Jan, 09, 2008 has been filed in this case.

Claim Objections

Claims 4-6 are objected to because of the following informalities:

The specification as originally filed only describes wherein said first conductive type semiconductor substrate is provided with having a first semiconductor substrate having said light-incident surface and a second semiconductor substrate bonded to said first semiconductor substrate and including side walls of said recessed portions.

Applicants' by substituting Having (first instance) with "comprises" to the extent they intend to claim other elements now the same is not supported by the specification as originally filed.

Claims 5-6 are objected to for at least depending upon objected to claim 4.

Appropriate correction is required.

Claim Rejections - 35 USC Section 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action.

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior ad are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,3-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mattson et al. (U.S. Patent No. 6,426,991, herein after Mattson) and Chappo et al. (U.S. Patent No. 6,510,195, herein after Chappo), both previously applied and further in view of Bauer et al. (U.S. Patent Application

Publication No. 2002/0011640, herein after Bauer, also cited by the Applicants).

With respect to claim 1 Mattson describes a back illuminated photodiode array comprising ; a first conductive type semiconductor substrate having a light-incident surface (Mattson figure 7 #64, fig. 12 # 142, abstract 4 th line from bottom).

Mattson describes an opposite surface but does not specifically mention a plurality of recessed portions located opposite said light incident surface.

However Chappo a patent from the same filed of endeavor describes in figures 2 to 4 # 52, 54 and 10, etc.#120 and col. 11 lines 4-8 describe an opposite surface with a plurality of recessed portions located opposite said light-incident surface to provide an electrical path from contacts on a back side of the photosensitive device through the substrate and the front and the back surfaces are aligned to each other.

Therefore it would have been obvious t o one of ordinary skill in the art at the time of the invention to include the an opposite surface with a plurality of recessed portions located opposite said light-incident surface instead of Mattson's opposite surface in Mattson's device. The motivation to make the afore mentioned substitution is to provide an electrical path from contacts on a

back side of the photosensitive device through the substrate and the front and the back surfaces are aligned to each other. (Chappo 2 lines 51-67 and col. 3 lines 1-12).

The remaining limitations of claim 1 are :

a plurality of spatially separated second conductive type semiconductor regions wherein one of said second conductive type regions is located at each bottom of said recessed portions; (Chappo col. 11 lines 5-8) wherein said second conductivity type semiconductor regions each individually constitute pn junction together with said first conductive type semiconductor substrate. (Mattson figure 3, Chappo col. 8 line 50-55).

Mattson and Chappo do not specifically describe the presently newly added limitation wherein said first conductive type semiconductor substrate is thinner in said recessed portions of said first conductive type substrate than in portions of said first conductive type semiconductor substrate located around said recessed portions.

However, Bauer, a patent from the same filed of endeavor, describes in figure 2 and paras 0016 and 0019 describe wherein said first conductive type semiconductor substrate is thinner in said recessed portions of said first conductive type substrate than in portions of said first conductive type

semiconductor substrate located around said recessed portions to match the areas of first and second diodes to a relationship with photon flows of the assigned wavelength regions at desired conditions to obtain desired properties including improved sensitivity for the shortwave region of the radiation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include Bauer's wherein said first conductive type semiconductor substrate is thinner in said recessed portions of said first conductive type substrate than in portions of said first conductive type semiconductor substrate located around said recessed portions in Mattson's and Chappo's device. The motivation for the said combination is to match the areas of first and second diodes to a relationship with photon flows of the assigned wavelength regions at desired conditions to obtain desired properties including improved sensitivity for the shortwave region of the radiation. (Bauer paras 0004, 005 and 0021).

With respect to claim 3 Mattson describes a back illuminated photodiode array according to claim 1, wherein said first conductive type semiconductor substrate is composed of a single semiconductor substrate. (Chappo Figure 2 A # 52, col. 6 lines6-8).

With respect to claim 4 to the extent entered Mattson describes a back illuminated photodiode array according to claim 1, wherein said first conductive type

semiconductor substrate comprises a first semiconductor substrate including said light-incident surface and a second semiconductor substrate bonded to said first semiconductor substrate and including side walls of said recessed portions. (Chappo col. 6 lines47-49, fig. 10 col. 1 lines 3-7).

With respect to claim 5 Mattson describes a back illuminated photodiode array according to claim 4, further comprising an etching stop layer existing between said first semiconductor substrate and said second semiconductor substrate and having resistance to a specific etching agent to be used for said second semiconductor substrate. (Mattson col. 5 lines 8-9, and Chappo col.6 lines 6-15, it is inherent for a stop layer to resistant the etching agent for second substrate in order for the stop layer to function as a stop layer).

With respect to claim 6 Mattson describes a back illuminated photodiode array according to claim 4, further comprising an insulation layer existing between said first semiconductor substrate and said second semiconductor substrate. (Chappo col. 7 lines 23-31, Mattson col .5 lines 24-25).

With respect to claim 7 Mattson describes a back illuminated photodiode array according to claim 1, comprising a plurality of electrode pads each formed on a top surface of each said frame pad and individually and electrically connected to each said second conductive type semiconductor region, respectively (Mattson col. 1 lines 31 to 57, Chappo col. 6 lines 12 to 19, col. 7 lines 35-48, figures 2 and 6).

With respect to claim 8 Mattson describes a back illuminated photodiode array according to claim 7, further comprising: an electric insulation layer formed on each said frame pad; (Chappo col. 7 lines 23-31, Mattson col.5 lines 24-25) and a conductive member formed on said electric insulation layer and electrically connecting said second conductive type semiconductor regions with said electrode pads. (Mattson col. 1 lines 31 to 57, Chappo col. 6 lines 12 to 19, col. 7 lines 35-48, figures 2 and 6).

With respect to claim 9 Mattson describes a back illuminated photodiode array according to claim 8, wherein said electric insulation layer is provided with a contact hole for connecting an end of said conductive member to said second conductive type semiconductor regions. (Chappo figure 10).

With respect to claim 10 Mattson describes a back illuminated photodiode array according to claim 1, where In each said second conductive type semiconductor region extends from the bottom of the respective recessed portion at which it is located to side surfaces of said respective recessed portion. (Chappo figure 10, col. 1 lines5-7).

With respect to claim 11 Mattson describes a back illuminated photodiode array according to claim 1: wherein each said second conductive type semiconductor regions extend from the bottom of the respective recessed portion at which it is located over side surfaces of said respective recessed portion to a top surface of the respective frame pad framing said respective recessed portion. (Chappo figure 9, col. 9 lines 60 - col. 10 line 20, Bauer fig.2 paras 0016, 0019, 0020).

With respect to claim 12 Mattson describes a back illuminated photodiode array according to claim 11, comprising: an electric insulation layer formed on each said frame part and having a contact hole opposing the top surface of each said frame part ; and electrode pads electrically connected to said second conductivity type semiconductor regions through each said contact hole. (Chappo figure 10, col. 10 line 30- col. 1 1 line 7).

With respect to claim 13 Mattson describes a back illuminated photodiode array according to claim 1, wherein each said frame part comprises a first conductive type separation region having higher impurity concentration than said first conductive type semiconductor substrate.(Chappo col. 12 line 47-49, as Chappo's semiconductor substrate described in col. 6 lines 6-8 is not doped and first conductive type separation region on frame is doped, the first conductive type separation region has higher impurity concentration than the substrate).

With respect to claim 14 Mattson describes a back illuminated photodiode array according to claim I wherein an opening' size of said recessed portions decreases with an increase in the depth of said recessed portions (well known in the art to decrease recessed portion, see Mattson figures).

With respect to claim 15 Mattson describes a back illuminated photodiode array according to claim 1 , wherein said light-incident surface side of said first conductive type semiconductor substrate is provided with a first conductive type accumulation layer having a higher impurity concentration than said first conductive semiconductor

substrate. (Chappo col. 12 line 47-49, as Chappo's semiconductor substrate described in col. 6 lines 6-8 is not doped and first conductive type separation region on frame is doped, the first conductive type separation region has higher impurity concentration than the substrate and fig. 14 ,vias and conductive type accumulation layer on first surface and co1.12 lines22-25).

B. Claim 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mattson et al. (U.S. Patent No. 6,426,991 , herein after Mattson) and Chappo et al. (U.S. Patent No. 6,510,195, herein after Chappo) and Bauer (U.S. Patent Publication No. 2002/0011640, herein after Bauer) as applied to claims 1-15 above and further in view of Yamanaka et al. (U.S Patent No. 6,372,558, herein after Yamanaka).

With respect to claim 16 Mattson describes a back illuminated photodiode array according to claim 4, wherein mutually opposing surfaces of said first semiconductor substrate and said second semiconductor substrate are different in their crystal plane orientation.

Mattson, Chappo and Bauer describe a back illuminated photodiode array according to claim 4 but do not specifically describe the first and the second semiconductor substrates to be in different in their crystal plane orientation.

However, Yamanaka in figure 8A and col. 13 line 60- col. 14 line 20 describes the first and the second semiconductor substrates to be in different in their crystal plane orientation to increase stability of the device increase productivity and enhance mechanical and electronic properties of the surface.

Therefore it would have been obvious to one of ordinary skill in the art at the

time of the invention to include Yamanaka's the first and the second semiconductor substrates to be in different in their crystal plane orientation In Chappo's device to increase stability of the device increase productivity and enhance mechanical and electronic properties of the surface.

C. Claim 26 is The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claim 26 is rejected under 35 U.S.C. 102(e) as being anticipated by and Chappo et al. (U.S. Patent No. 6,510,195, herein after Chappo).

With respect to Claim 26 Chappo describes a back-illuminated photodiode array (col.5 line 34) comprising a semiconductor substrate , wherein only one side of said (col. 6 line 18) semiconductor substrate has a plurality of recesses (col. 11 lines 4-6) , and wherein each shape of openings of said recesses is square.(figs. 2b and 17 similar to Applicants' figure 1, see also col.6 line 39-46, col. 13 line 29-41, col.2 line 49-54 square sub module 22 fits in recess of similar shape).

Response to Arguments

Applicant's arguments filed on 02/06/2008 have been fully considered but they are not persuasive for the following reasons :

Applicants' have not set out specific reasons that can be responded .

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN H. RAO whose telephone number is (571)272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Steven H Rao/
Examiner, Art Unit 2814